符号	訂正年月日	記号	訂正記事	担当	承認
1	57・2・3	A	D9~12 10E2 追加(過入力による Tr 保護)	大多	スガ
2	57・4・13	B	R71.72 23.1K → 23.3K 変更	大多	中山

安全規格			登録者名	
規格名	区分		登録番号	表

TP1

TP3

+85V +50mA

-85V -50mA

TP2

TP4

TRANSISTORS

Q1.2	2SK147
Q3.4	2SJ72
Q9.10.15.16.27.28.29.30.31.32.35.96.37.38	2SC2602
Q61.62.67.68.79.80.81.82.83.84.87.88.89.90	2SC2602
Q11.12.13.14.21.22.23.24.25.26.33.34.39.40	2SA1114
Q63.64.65.66.71.72.73.74.75.76.85.86.91.92	2SA1114
Q5.6.19.20.41.42.45.46.49.50.53.54	2SC1904
Q57.58.77.78.93.94.95.96.99.100.103.104	2SC1904
Q7.8.17.18.43.44.47.48.51.52.55.56	2SA899
Q59.60.69.70.97.98.101.102.105.106.107.108	2SA899

DIODES

D1.2.3.4.5.6.7.8	10DA2
Ⅲ D9.10.11.12	10E2

CAPACITORS

NON MARK ; MICRO FARAD
Ⓜ ; MICA
P ; PICO FARAD
⫩ ; ELECTOROLYTIC
(NP) ; NON POLA
(SP) ; PS. PP FILM CAPACITOR

RESISTORS

NON MARK ; OHM
K ; KILO OHM

LAST NO.	Q	D	C	R
	108	12	24	158

Ⅲ

VACANT	Q	D	C	R

E-704

品番	部品番号	部品名	個数	材質	処理	板厚	材料メーカ名	CAT.No	UL フレームクラス	HW1 (秒)	HAAI (図)	製造番号

承認	照査	検図	設計	適用		名称	AMF-057 EQ アンプ Ass'y
	56・11・5	56・11・5	56・10・31	尺度	C-Zla		
電野	西山	中山	K. Sasaki	単位	普通寸法公差 以下± 以下± 以下± テコエ±	部番	EQ Amp Ass'y
パイオニア株式会社						整番	ZAX8441B

4. 回路概要

今日，高度に発達したNFB技術によりアンプの諸特性はめざましく向上しています．しかし，NFBアンプは出力信号の一部を入力段に戻し，入・出力波形が相似になるように補正しているため，TIMひずみ(動的ひずみ)を発生するメカニズムを持っています．TIMひずみを根本的に無くするにはNFBをかけないことですが，NFBによる諸特性の改善は多大なものがあり，S/Nやひずみが非常に不利になります．特に増幅素子として使用されるFETやトランジスタは，元来非直線特性の素子であり，これを解決しないかぎりNon NFBアンプはNFBアンプに太刀打ちできません．

C-Z1は，FETやトランジスタなどの持つ"半導体固有の非直線性を，逆モードの非直線性により完全に吸収してしまう"という発想により開発したスーパーリニアサーキットを採用したNon NFBアンプ(注)です．NFBによる諸特性の改善が無いため，高級部品を厳選して使用し，配線材やそのスタイリングについても十分に検討しています．

注．
ここでいうNon NFBとは電圧帰還ループを持たないということです．FETやトランジスタなどは自己帰還を行う電流帰還素子ですから必ず電流帰還がかかります．しかし，素子の内部抵抗やその延長とみなせるエミッタ抵抗による電流帰還はTIMひずみとは全く関係なく，音質や特性への影響はありません．

スーパーリニアサーキット

スーパーリニアサーキットは，半導体増幅素子の持つ個有の非直線性を逆モードの非直線性により完全に吸収し，等価的に優れた直線性を実現する回路です．

図4-1によりその原理を説明します．Q4のコレクタ電流Ic_1とQ5のコレクタ電流Ic_3は，Q3のコレクタ電流Ic_2と等しくなります(ただし，R1＝R2＝R3とする)．今，Q1のベースに入力電圧Viが加わったとすると，Q2のエミッタ電圧Vaは次式で示されます．

$$Va = Vi + V_{BE1} - V_{BE2} \quad \cdots\cdots(1)$$

Q1とQ2の特性が揃っていれば，V_{BE1}とV_{BE2}は等しくなり，V_{BE}の項が消えてしまいます($Ic_1 = Ic_2$)．

$$Va = Vi \quad \cdots\cdots(2)$$

また，Ic_2は次式で示されます．

$$Ic_2 = \frac{Va}{R_E} = \frac{Vi}{R_E} = Ic_3 \quad \cdots\cdots(3)$$

出力電圧Voは次式で示されます．

$$Vo = Ic_3 \cdot R_L = \frac{Vi}{R_E} \cdot R_L = \frac{R_L}{R_E} \cdot Vi \quad \cdots(4)$$

したがって，出力電圧は入力電圧のR_L/R_E倍となり，非直線要素(V_{BE})は消えてしまいます．

実際の回路ではQ1，Q2のコレクタ損失を均一にしたり，プッシュプル化して2電源にするなどしており，さらにスーパーリニアサーキットをアルミケース内にエポキシ樹脂で充填してモジュール化し，熱的安定性やシールド効果を改善して信頼性を向上させています．

図4-2にスーパーリニアサーキットモジュール(AXX-002)を使ったフラットアンプを示します．モジュール内の初段は，FETとトランジスタのカスケード接続によるプッシュプルのソースホロワバッファアンプです．2段目以降はコンプリメンタリのスーパーリニアサーキットです．出力段はモジュール外の純A級SEPP回路です．

カレントイコライザー

スーパーリニアサーキットは，前に述べたように負荷抵抗(R_L)の値により利得が決まります(R_Eを一定とする)．そこで，この特徴を生かし，負荷にRIAA特性を持ったインピーダンスを使用することにより，イコライザーを構成することができます．

図4-3はC-Z1のイコライザー部の構成を示します．CR型イコライザーのように見えますが，根本的な違いはCR型イコライザーが一度大きく増幅したものを減衰させているのに対し，カレントイコライザーではアンプ自体の利得が高域で抑えられるため，高域のクリップマージンを大きくすることができます．RIAA特性を低域上昇と高域下降に分けているのは，直流域の安定化とひずみ低減などの必要からです．

ダブルロックド・サーボレギュレータ

Non NFBアンプは出力点のDC電圧の安定化が非常に重要となります．

図4-4はC-Z1で採用した"ダブルロックド・サーボレギュレータ"の基本構成を示します．この方式は，一度安定化した電源を中点電位の検出により制御される安定化回路を通じて供給するものです．この方式は一般DCサーボ方式と異なり，信号系に直接サーボループが構成されないため，Non NFBアンプの特長を生かすことができ，さらに全段直結化を実現します．

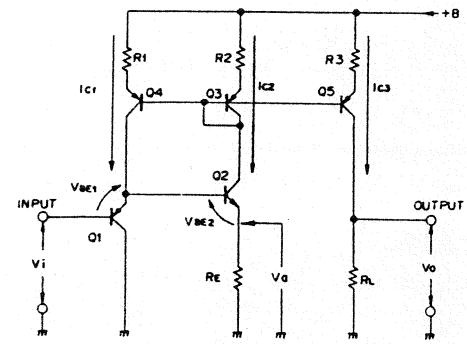

図4-1 スーパーリニアサーキット基本回路

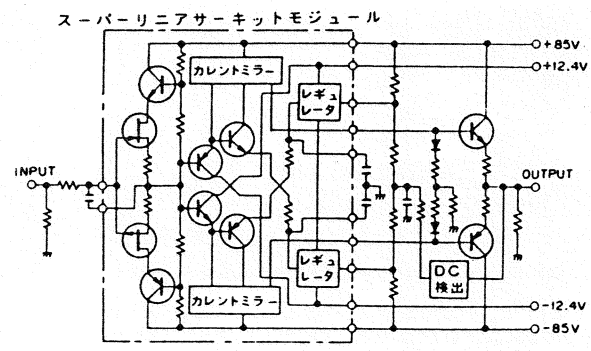

図4-2 スーパーリニアサーキットモジュールを使用したフラットアンプ

Adjustment of power supply voltage (±85 V ±0.5 V)

* Before turning on switch for power supply assembly (A), Turn VR1 and VR4 fully clockwise and the VR2 and VR3 fully counter clockwise.

A) Point of measurement, B) Point of adjustment, C) Specifications, D) Notes, E) Check, F) Check, G) Check, H) Approximately DC 70 V, I) Approximately DC 85 V, J) Adjusting both should give a reading within ±0.5 V of the voltage's absolute value. K) Approximately DC 85 V, L) Adjusting both should give a reading within ±0.5 V of the voltage's absolute value, M) Rear panel, N) Power supply assembly (A)

4. OUTLINE OF CIRCUITS

Today, the performance characteristics of amplifiers have reached a new high because of the rapid developments in NFB (negative feed back technology). Because part of the NFB amplifiers's output goes back to the input stage, compensation must be made for the fact that the output and input wave forms are different. Consequently, a source of TIM (Transient intermodulational distortion or dynamic distortion) exists. TIM can be eliminated by not using NFB, but many characteristics improve with NFB although S/N & distortion

do not. With FET's and transistors being used as amplification elements, unless something is done to compensate for this due to their non linearity characteristics, NFB will be superior to non NFB devices.

The C-Z1 is a non NFB amplifier (see note) which uses a superlinear circuit based on the concept of absorbing the non linear characteristics of FET's and transistors with a reverse non linearity mode. Because the improvements of characteristics that accompany NFB are not present, quality parts have been carefully selected and wiring material and positioning have been given thorough consideration.

Note: The term non NFB used here refers to the fact that a voltage feedback loop is not used. Although FET and transistors are a type of element effecting current feedback on their own, current feedback does not exist. However, the current feedback resulting from the elements internal resistance plus that developed by the emitter has no relation to TIM distortion and has no influence on sound quality characteristics.

Super linear circuit

The super linear circuit by using a reverse mode non

linearity completely absorbs that non linearity of the semi conductor amplifying elements resulting in superior linearity characteristics. This theory is explained in figure 4-1. The current from the Q4 collector, IC1 and Q5 collector current IC3 become the same as the current IC2 from the Q3 collector. (That is to say that R1 = R2 = R3) If the voltage Vi is input to the base of Q1, the Q2 emitter voltage Va is as shown in the formula below.

$$Va = Vi + Vbe1 - Vbe2 \quad (1)$$

If Q1 and Q2 are the same, Vbe1 and Vbe2 become equal and the term Vbe becomes equal to zero (IC1 = IC2).

$$Va = Vi \quad (2)$$

IC2 is as shown in the following equation.

$$IC2 = Va/Re = Vi/Re = IC3 \quad (3)$$

The output voltage Vo is as shown in the following.

$$Vo = IC3 \times R1 = (Vi/Re) \times R1 = (R1/Re) \times Vi \quad (4)$$

That is to say, the output voltage becomes (R1/Re) times the input voltage. The voltage Vbe (non linearity element) disappears.

In the actual circuit, the collector losses of Q1 and Q2 are made equal, a double push pull type power source is included, the super linear circuit is encased in an aluminum case bonded with epoxy resin to make a

module. The heat characteristics and effectiveness of the shielding is improved to increase reliability.

The flat amp used in the super linear circuit module (AXX-002) is as shown in figure 4-2. The first stage in the module is a push-pull source follower buffer amplifier attached to the FET and transistor cascade. The second stage and above consists of the complimentary super linear circuit. The output stage is outside of the module and consists of a pure class A SEPP (single ended push-pull) circuit.

Current equalizer

For the super linear circuit, it was shown above that its gain was decided by the value of the load resistance (Rl) assuming that Re remains fixed. If an impedence having RIAA load characteristics is used to enhance the above features, it will be possible to include an equalizer in the circuitry.

The equalizer section included for C-Z1 is as shown in figure 4-3. It appears to be a CR type equalizer but the difference is that while a CR type equalizer will decrease the previously amplified current, the current gain equalizer will increase the creep margin in the high ranges that the amplifier itself tends to suppress.

It is necessary to divide RIAA characteristics into increasing low levels and decreasing high levels in order to gain stability in the rectifying current and to decrease distortion.

Double locked servo regulator

For non NFB amplifiers, the stability of output DC voltage is extremely important. The plan for the double locked servo regulator used in the C-Z1 is as shown in figure 4-4. In this method, the voltage supply is monitored at a point of mid potential and this results in a current being fed back to the stabilizer control circuit to further control the voltage supply. This is different from the normal DC servo method in that there is no servo loop included in the signal circuit and that the special characteristics of the non NFB amplifier can be attained by doing everything in a direct fashion.

A) Figure 4-1 Basic super linear circuit, B) Super linear circuit module, C) Current mirror, D) Regulator, E) Regulator, F) Current mirror, G) DC detection, H) Figure 4-2 The flat amp using the super linear circuit module

Output buffer amplifier

The input stage with a source follower push pull

circuit based on FET's and transistor cascade is a fixed current load.

The output stage is a pure class A SEPP as the DC voltage at the output midpoint is checked and the fixed current source is controlled thus keeping the output midpoint at zero potential.

A) Current equalizer load (Raises lower values), B) Equalizer filter (Lowers higher values) C) Super linear circuit module, D) Super linear circuit module, E) Bias circuit, F) Bias circuit, G) Figure 4-3 Schematic for the current equalizer, H) Super linear circuit, I) DC detection circuit, J) Power transformer, K) Rectifier circuit, L) Stabilized fixed voltage supply, M) Stabilized fixed voltage supply, N) Figure 4-4 Basic plan for double locked servo regulator, O) DC detection circuit, P) Figure 4-5 Schematic for the buffer amplifier, Q) Equalizer amplifier, R) Flat amplifier, S) Buffer amplifier, T) Figure 4-6 Layout of relays

Other (The signal system)

* Changing of cartridge load

The input resistance and capacity for the phono circuit can be changed in three different stages, allowing adapting to the cartridge load characteristics.

* Phono sub sonic filter

If the function switch is put on PHONO SUBSONIC, the Cr filter (fc = 15 Hz, -6 dB/oct) part of the equalizer circuit is connected cutting out very low frequencies.

* Volume control

A high quality 4 step switch is used improving S/N by controlling output.

* Tone control

Tone can be controlled by using a fixed loss of -3 dB Cr tape from BASS (50 Hz) to TREBLE (20 kHz) in 1.5 dB steps with a variation of ±3 dB. When the TONE is off, the signal passes through a -3 dB attenuator.

Relay control logic circuit

In the operation part of the C-Z1, feather touch tactile switches are employed, with the signal circuit relays being controlled by the logic circuits. Figure 4-6 shows the position of the relays while operating. Figure 4-7 shows the control circuits for the relays. The figure shows Q1 composed of a CMOS digital IC which has four pairs of built in clocked D latches. Q2 is composed of CMOS digital IC's which have two pairs of built in J-K flip flops. Q3 and Q4 are composed of digital IC's (Not circuits) having seven NPN Darlington transistors and with just a small input, large values of current can be switched. (400 mA max). For the

function changing circuit, (TUNER, AUX, PHONO, PHONO SUBSONIC) a D latch is utilized which permits selecting the desired operation. The D latch fixes the value of the output signal to that of the clock pulse signal which enters (either L or H). Afterwards, even if the input should change, the output will not change.
When the function button is pushed, it is detected that D1-D4 & C9 change from L to H and clocked pulse input into D latch. Because the D latch in the circuit of the button pushed has an H level input, the output is set at H level. Because the others have a low level input, the output is set at L level. The D latch being a H level output circuit and in order to make the next stage's Not gate output L level (NPN transistor is on) the circuit relays operate; the indicator lamps are illuminated.

For the TONE and TAPE MONITOR circuits, pushing the relevent button will input into the flip flop terminal (CK) at which time the flip flop will reverse. When the output of the flip flop is H level, the NOT gate output (Q) in the next stage will be L level (NPN transistor is on), the relays will operate and the indicator lights will be illuminated.

A) D30-37 Signals and root indicators, B) Figure

4-7 Relay control logic circuit

* Output muting

There is muting capacity (ground type) used for preventing transient noises when turning the C-Z1 on and off.

When the power is switched on (See figure 4-7) Q12 receives load voltage from D40 and D41 and is switched off, C1 is charged and Q9's base voltage is raised. After about 22 seconds, Q8 and Q9 are switched on and the output muting relay RL 8 (at brake) operates, and muting (output circuit ground) is terminated. With the charging of C2 in about 20 seconds, (about 2 seconds before muting is cancelled, Q10, Q11 and Q7 are switched on and the relays in the signal circuit operate and the signal root indicator LED is illuminated.

When power is turned off, Q12 is switched on by the residual power because the reverse bias quickly disappears, Q7-Q11 go off and all relays are released (except for RL6 and RL7) and the muting condition is resumed.

* Memory for switch position

Because the D latch and flip flop IC's are of the CMOS type, a small amount of current (in micro amps.)

is sufficient to preserve their contents. The backup current for these IC's is furnished by a 2.5 F condenser (4 x 10 F capacitors) and even if the AC current is cut off for 3 days or more, the switch position information is preserved.

*Reset/Preset circuit

If the back up time is exceeded on the above mentioned condenser, the button switch positions will resume their starting position when the current is again turned on. In order to recharge the backup condensers (C12-C15) when the power is turned on, the Q5 emitter voltage is temporarily lowered, passing through R42 and D26, the Q6 voltage is reduced and Q6 is temporarily switched on. Because of this, the Q6 collector voltage rises, the reset pulse passes through C11 and is supplied to the D latch and flip flops. Output Q becomes L level and the Tone and TAPE MONITOR are put in off position.The reset pulse is input into the clock terminal of the D latch and also passes D11 of the turner circuit and inputs into the data terminal. As a result, only this circuit's D latch is set at H level and becomes the TUNER function.